Notice of References Cited	Application/Control No. 09/915,437	Applicant(s)/Patent Under Reexamination DHONG ET AL.	
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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
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FOREIGN PATENT DOCUMENTS

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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Yee et al., "Dynamic Logic Synthesis," IEEE. Jan 1997, pp. 345-348
	V	Puri et al. "Logic Optimization by Output Phase Assignment in Dynamic Logic Synthesis" IEEE 1996, pp 2-8.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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